CLAIMS

1. (Currently Amended) A logic circuit comprising:

a combinatorial logic having at least first and second input signal lines and at least a first output signal line; and

a shift register latch (SRL) chain and a last SRL within the SRL chain, connected to the output of the combinatorial logic, a first SRL of the SRL chain being connected to the first input signal line for outputting a first scan signal thereto, a second SRL of the SRL chain being connected to the second input signal line for outputting a second scan signal thereto, the last SRL being connected to the first output signal line for receiving a first output signal of the combinatorial logic; and

a logic unit having at least first and second logic input lines and a logic output line, the first logic input line being connected to the first SRL for receiving the first scan signal therefrom, the second logic input line being connected to a pattern adjust line for receiving a control signal, the logic output line being connected to the second SRL for outputting a logic output signal thereto, wherein the logic output signal is at least one of the first scan signal and an inverted signal of the first scan signal, depending on the logic value of the control signal.

2. (Original) The logic circuit of Claim 1, wherein the logic unit comprises an XOR gate having the first and second logic input lines and the logic output line.

3. (Original) The logic circuit of Claim 1, wherein the logic output signal is the first scan signal when the control signal is a logical 0, and is the inverted signal when the control signal is a logical 1.

4. (Original) The logic circuit of Claim 1, wherein each of the SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line.

5. (Currently Amended) The logic circuit of Claim 1, wherein each SRL of SRL latch chain and the last SRL within the SRL chain, comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line, wherein the master latch is synchronized to a data clock signal on the data clock line for receiving and temporarily storing a logic data bit through the data input signal line, wherein the master latch is synchronized to a scan clock signal on the scan clock line for receiving and temporarily storing a scan data bit through the scan input signal line, and wherein the slave latch is synchronized to a slave clock signal on the slave clock line for receiving and temporarily storing at least one of the logic data bit and the scan data bit from the master latch.

6. (Currently Amended) A method for enhancing test coverage in a level-sensitive scan design (LSSD), the method comprising the steps of:

receiving a first scan data bit by a first SRL;

temporarily storing the first scan data bit in the first SRL;

transmitting the first scan data bit from the first SRL to a logic unit;

transmitting the first scan data bit from the logic unit to [[the]] a second SRL if there is ~~not~~ a logic [[1]] 0 control signal;

temporarily storing the first scan data bit in the second SRL;

~~transmitting an inverted bit of the first scan data bit from the first SRL to the logic unit;~~

transmitting an inverted bit of the first scan data bit from the logic unit to the second SRL if there is ~~not the~~ a logic 1 control signal;

temporarily storing the inverted bit in the second SRL;

receiving a second scan data bit by the first SRL;

temporarily storing the second scan data bit in the first SRL;

transmitting the first scan data bit from the second SRL to a combinatorial logic, and the second scan data bit from the first SRL to the combinatorial logic;

transmitting the inverted bit from the second SRL to the combinatorial logic, and the second scan data bit from the first SRL to the combinatorial logic;

receiving a first output data bit of the combinatorial logic by a last ~~third~~ SRL within the SRL chain, the first output data bit being output from the combinatorial logic receiving at least the first and second scan data bits in response to a logic 0 control signal;

temporarily storing the first output data bit in the last ~~third~~ SRL;

receiving a second output data bit of the combinatorial logic by [[a]] the last ~~third~~ SRL within the SRL chain, the second output data bit being output from the combinatorial logic receiving at least the inverted bit from the second SRL and the second scan data bit in response to a logic 1 control signal;

temporarily storing the second output data bit in the last ~~third~~ SRL; and

enhancing test coverage of the combinatorial logic by obtaining both the first and second output data bits from the last ~~third~~ SRL.

7. (Currently Amended) The method of Claim 6, wherein the step of transmitting the ~~an~~ inverted bit of the first scan data bit from the logic unit to the ~~a~~ second SRL further comprises the step of XORing ~~the inverted bit of~~ the first scan data bit with the logic 1 control signal.

8. (Currently Amended) The method of Claim 6, wherein each of the first, second, and last ~~third~~ SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line.

9. (Currently Amended) The method of Claim 6, wherein each of the first, second, and last ~~third~~ SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line, wherein the master latch is synchronized to a data clock signal on the data clock line for receiving and temporarily storing a logic data bit through the data input signal line, wherein the master latch is synchronized to a scan clock signal on the scan clock line for receiving and temporarily storing a scan data bit through the scan input signal line, and wherein the slave latch is synchronized to a slave clock signal on the slave clock line for receiving and temporarily storing at least one of the logic data bit and the scan data bit from the master latch.

10. (Currently Amended) A method for enhancing test coverage in a level-sensitive scan design (LSSD), the method comprising the steps of:

receiving and temporarily storing a first scan data bit;

transmitting the first scan data bit from a first SRL through a logic unit to a second SRL if there is ~~not~~ a logic [[1]] 0 control signal;

receiving and temporarily storing a second scan data bit;

generating an inverted bit of the first scan data bit if there is a logic 1 control signal;

generating a first output data bit by receiving the first and second scan data bits;

transmitting the first output data bit to a last SRL within the SRL chain;

generating a second output data by receiving the inverted bit and the second scan data bit;

transmitting the second output data bit to the last SRL within the SRL chain; and

enhancing test coverage of combinatorial logic by obtaining both the first and second output data bits.

11. (Cancelled)